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Wideband cryogenic amplifier for a superconducting nanowire single-photon detector*

Lianming LI[†‡1, 2], Long HE[2], Xu WU[1,2], Xiaokang NIU[1], Chao WAN[2], Lin KANG[2,3], Xiaoqing JIA[2,3], Labao ZHANG[2,3], Qingyuan ZHAO[2,3], Xuecou TU[2,3]

[1]*National Mobile Communications Research Laboratory, Department of Radio Engineering, School of Information Science and Engineering, Southeast University, Nanjing 210096, China*

[2]*Purple Mountain Laboratories, Nanjing 211111, China*

[3]*Research Institute of Superconductor Electronics, School of Electronic Science and Engineering, Nanjing University, Nanjing 210093, China*

[†]E-mail: Lianming.LI@seu.edu.cn

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Abstract: We present a low-power inductorless wideband differential cryogenic amplifier using a 0.13-μm SiGe BiCMOS process for a superconducting nanowire single-photon detector (SNSPD). With a shunt–shunt feedback and capacitive coupling structure, theoretical analysis and simulations were undertaken, highlighting the relationship of the amplifier gain with the tunable design parameters of the circuit. In this way, the design and optimization flexibility can be increased, and a required gain can be achieved even without an accurate cryogenic device model. To realize a flat terminal impedance over the frequency of interest, an RC shunt compensation structure was employed, improving the amplifier's closed-loop stability and suppressing the amplifier overshoot. The *S*-parameters and transient performance were measured at room temperature (300 K) and cryogenic temperature (4.2 K). With good input and output matching, the measurement results showed that the amplifier achieved a 21-dB gain with a 3-dB bandwidth of 1.13 GHz at 300 K. At 4.2 K, the gain of the amplifier can be tuned from 15 to 24 dB, achieving a 3-dB bandwidth spanning from 120 kHz to 1.3 GHz and consuming only 3.1 mW. Excluding the chip pads, the amplifier chip core area was only about 0.073 mm^2.

Key words: Cryogenic amplifier; Wideband amplifier; Superconducting nanowire single-photon detector (SNSPD)
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1 Introduction

Given its wide spectral response over the visible to infrared range, and rapid and reliable detection, the superconducting nanowire single-photon detector (SNSPD) has a wide range of applications, such as quantum key distribution for quantum communication, free-space optical communication, integrated circuit defect detection, spectrum measurement, and radiation detection (Tarkhov et al., 2008; Birnbaum et al., 2011; Marsili et al., 2013; Kitaygorsky et al., 2017; Liu et al., 2017; Debnath et al., 2019). Fig. 1a shows a typical SNSPD readout system. As indicated there, and considering the implementation issues, e.g., the DC operating point of the readout amplifier and SNSPD, a readout amplifier is usually connected through a large capacitor with the SNSPD to realize photon sensing and amplification. Through a long coaxial cable line, the output signal from the readout amplifier can be measured with external equipment or other circuits. With the help of liquid helium in a special Dewar or refrigerator, the SNSPD with a load

‡ Corresponding author
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ORCID: Lianming LI, https://orcid.org/0000-0003-1873-4806
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resistor R_L and the readout amplifier are put in a cryogenic environment with a temperature lower than 4.2 K. In this way, a long wire between the quantum devices and the readout amplifier can be avoided, and the readout amplifier can be put as close as possible to the SNSPD devices, realizing a compact readout system. In addition, system sensitivity is enhanced, as the device has lower noise at cryogenic temperature (Bardin and Weinreb, 2008; Montazeri et al., 2016) and wire insertion loss and system size are reduced.

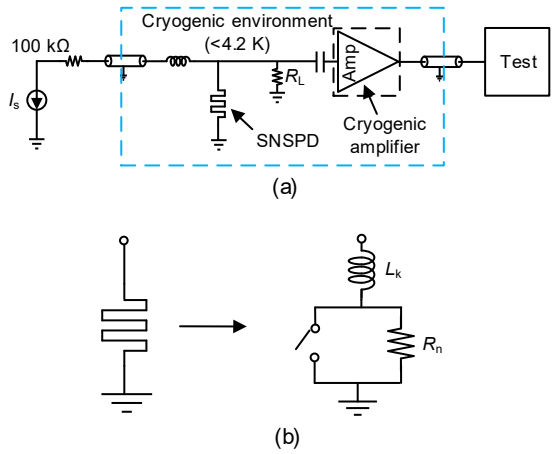

Fig. 1 A typical superconducting nanowire single-photon detector (SNSPD) readout system (a) and the equivalent electrical model of the SNSPD (b)

In Fig. 1, the SNSPD is biased by a current source and a resistor with a typical value of 100 kΩ. Note that the loading resistor R_L is set at 50 Ω. In principle, this R_L provides a path to discharge the biasing current of the SNSPD (Yamashita et al., 2010). Accordingly, the latch-up effect, which is caused by inherent eddy current, noise, thermal fluctuation, and continuous photon triggering in a short period of time, can be effectively suppressed, ensuring a reliable operation of the SNSPD. To analyze the SNSPD, the equivalent model shown in Fig. 1b can be used for convenience. As indicated, it consists of an inductor L_k, a resistor R_n, and a switch in parallel with R_n. Normally, the SNSPD is in a superconducting mode, and the switch is on, leading to near 0 Ω DC resistance. In contrast, when the SNSPD absorbs a photon, the switch opens and the SNSPD behaves as having a high resistance. In this way, the current in the SNSPD is forcibly injected to the load resistor R_L, thereby generating a voltage pulse signal, which is the signal to be measured by the readout circuit. As illustrated, Fig. 2 shows our normal measured SNSPD transient results. With a 52-dB room temperature amplifier, its output signal amplitude is around 120 mV, translated into an about 300-μV output amplitude of the SNSPD. As indicated, its rising time is about 100 ps, while its falling time is about 50 ns. Recently, in Tao et al. (2020), with 5-nm-thick NbN film, the SNSPD achieved a system detection efficiency (SDE) of 68% at 1550 nm and a low dark count rate (DCR) of 1 Hz.

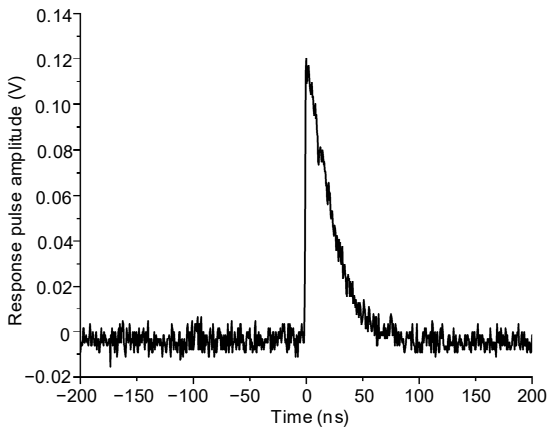

Fig. 2 Amplified response of the superconducting nanowire single-photon detector (SNSPD) at room temperature

Clearly, as the SNSPD's output signal amplitude is very small, as an interface to the SNSPD device, the cryogenic readout amplifier is an indispensable part of the above-mentioned compact SNSPD readout system. However, because of the critical cryogenic working environment and above-mentioned SNSPD characteristics, the design of the cryogenic amplifier faces several challenges in implementation.

First, the cryogenic amplifier's power consumption should be very low. For future SNSPD multi-pixel applications, the SNSPD array is needed to increase the photon number and the time and spatial resolution. As a result, a large number of cryogenic amplifiers are required. However, the cooling power of a typical closed-cycle cooler is very limited, and this sets the maximum allowed power consumption of the cryogenic electronics at around 1.5 W at 4.2 K (SHI Cryogenics Group, 2012).

Secondly, in the commercial foundry process, the cryogenic device model is lacking, making it very difficult to realize accurate circuit design. Typically,

III-V devices, such as indium phosphide (InP), high electron mobility transistors (HEMTs), and silicon germanium heterojunction bipolar transistors (SiGe HBTs), can be used for cryogenic amplifiers, showing remarkable performance of high speed and low noise (Cahall et al., 2016; Ramírez et al., 2019). Among them, the InP HEMT cryogenic amplifier typically has better performance and lower power consumption than the SiGe HBT one, but its integration level is very low (Qu et al., 2019; Cha et al., 2020). In contrast, the SiGe HBT cryogenic amplifier has the advantages of low fabrication cost and high integration level. In addition, it provides CMOS devices. As a result, SiGe HBT is preferred over III-V devices to realize a flexible, compact, and low-cost SNSPD system. However, the lowest valid temperature of the foundry SiGe device model is only about −40 °C, which is very far from the 4.2 K cryogenic temperature. So, how to optimize and evaluate the cryogenic amplifier performance in its design and test stages becomes a big challenge.

Thirdly, to achieve high-fidelity pulse amplification, a cryogenic amplifier should have wide bandwidth and high gain. For simulation and test, avoiding signal overshoot and SNSPD oscillation, and considering the system implementation, the low cut-off frequency of the cryogenic amplifier should be around 100 kHz. Moreover, to secure the SNSPD signal energy, signal-to-noise ratio (SNR), and edge performance, and to detect very weak photonic signals with low power consumption, the high cut-off frequency and gain of the amplifier should be around 1 GHz and 20 dB, respectively. Note that, with a 20-dB gain, the amplifier's typical output signal amplitude is about 3 mV, which is high enough for the following signal to proceed.

In the past decade, several SiGe HBT cryogenic amplifiers have been reported (Moschetti et al., 2012; Schleeh et al., 2013), but they all consume more than 4 mW power. In Wong et al. (2020), a SiGe low-noise amplifier (LNA) was demonstrated with a more than 25 dB gain over a 4–8 GHz bandwidth. This LNA consumes only 1 mW. However, it is not suitable for SNSPD readout application, as the main signal energy of an SNSPD typically falls in the frequency range from DC to 1 GHz. To improve the bandwidth, Bardin and Weinreb (2010) used an on-chip spiral inductor, with the penalty of large chip area and high cost. He et al. (2019) produced a compact two-stage inductorless wideband SNSPD readout amplifier with an emitter follower and a Cherry-Hooper amplifier, which consists of a transconductance stage and a transimpedance gain stage. At 4.2 K, the amplifier achieved a 3-dB bandwidth of 130 kHz–3.4 GHz and a 23-dB gain with a power consumption of 4 mW. Note that the bandwidth of this amplifier is higher than the SNSPD requirement, but it introduces more noise and has a relatively high power consumption. As a result, for future SNSPD multi-pixel applications, it is still desirable to explore power- and area-efficient wideband cryogenic amplifier design techniques.

To address the above issues, with the low-power wideband gain topology and shunt–shunt feedback mechanism, in this study a compact low-power wideband cryogenic amplifier is proposed for SNSPD readout applications without using any inductor. With benefits of high integration and good radio frequency (RF) performance, a SiGe HBT process is employed. To solve the issue of lacking the cryogenic device model and to realize a low variance of the terminal impedance over the frequency range of interest, a capacitive coupling and an RC shunt compensation structure are employed. Theoretical analysis and simulations have been undertaken, highlighting the relationship of the amplifier gain performance with the tunable design parameters of the circuits and increasing the amplifier design and optimization flexibility. With a 0.13-μm SiGe process, the proposed amplifier has a low cut-off frequency of 120 kHz, a measured gain of over 20 dB, and a high cut-off frequency of more than 1.3 GHz, consuming only 3.1 mW power at 4.2 K. Excluding the chip pads, the amplifier's chip core area is only about 0.073 mm^2.

2 Amplifier design

2.1 Amplifier topology

Fig. 3 shows the proposed low-power wideband cryogenic amplifier structure. As indicated, the amplifier consists of an input amplifier stage, an emitter follower output buffer stage, and a shunt–shunt feedback stage. Different from He et al. (2019), in this design the emitter follower output buffer is combined in the input amplifier stage, thereby driving the test equipment and realizing the shunt–shunt feedback to achieve the required 50-Ω impedance for input impedance matching and to increase the bandwidth

performance. To solve the above-mentioned problem of lacking a cryogenic device model, two circuit topology schemes are employed. First, the buffer is AC-coupled to the input amplifier with two capacitors C_1 and C_2. In this way, not only the DC-offset voltage generated by the input amplifier is eliminated, but also an independent DC biasing point can be realized. Accordingly, the design and optimization flexibility are increased and the potential device performance can be explored, making it possible to achieve good circuit performance at different temperatures. Note that the amplifier's low cut-off frequency is determined mainly by the coupling capacitors C_1 and C_2. Simulations show that, with a larger capacitor value, the amplifier's low cut-off frequency will decrease. However, because of the parasitic capacitances of C_1 and C_2, the amplifier's high cut-off frequency will also decrease. In this design, considering their effect on the amplifier's low and high cut-off frequencies, the coupling capacitors C_1 and C_2 are optimized, and we set the amplifier's low cut-off frequency at around 120 kHz. Secondly, the input and output buffer stages are biased with a tail current and a current mirror correspondingly, realizing a fully differential topology. In this way, well-defined device DC operating points can be obtained over different temperatures. This also has the benefits of suppressing the common-mode noise and minimizing the impact of the off-chip parasitic inductor. This can improve the circuit reliability and performance.

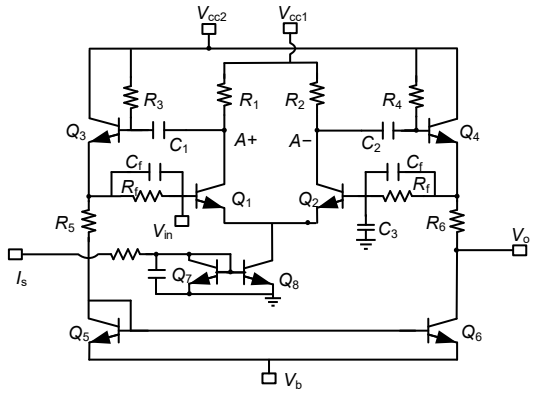

Fig. 3 Schematic of the wideband cryogenic amplifier

To be specific, as shown in Fig. 3, the input amplifier stage has a resistively loaded common-emitter (CE) amplifier configuration. To achieve a trade-off among gain, bandwidth, noise, and power consumption, the component values of input transistor Q_1 and load resistor R_1 are optimized. As mentioned, the current of Q_1 is provided by a tail current, which is realized by a current source with a current mirror of Q_8 and Q_7. With the differential emitter–follower pair Q_3 and Q_4 and its current mirror load pair Q_5 and Q_6, a differential to single-ended output conversion is realized. Here, resistors R_5 and R_6 are added to provide a broadband output match to 50 Ω for testing. As reported in Russell and Weinreb (2012), the transistor's turn-on voltage increased from 0.65 to 1 V. To increase the amplifier voltage headroom, the bases of transistors Q_3 and Q_4 are connected to a supply voltage V_{cc2} through two bias resistors R_3 and R_4. The emitters of transistors Q_5 and Q_6 are biased by biasing voltage V_b to realize an optimal biasing point of Q_1 and Q_2 over a large temperature range, thereby achieving optimum device performance.

As will be discussed shortly, to illustrate the amplifier's working principle and performance optimization, the small-signal model of the amplifier is analyzed, highlighting the relationship of the amplifier gain with tunable design parameters, such as biasing current. In this way, even without an accurate cryogenic device model, a required gain can be realized. In addition, capacitor C_f is added in parallel with R_f to compensate for the phase shift, thus improving the amplifier's closed-loop stability and suppressing the amplifier overshoot and ringing.

2.2 Small-signal model analysis

To simplify the calculation, Fig. 4 shows the amplifier's single-ended half circuit and its small-signal model. Note that this circuit does not take into account the current mirror load of the output buffer, as it has less effect on the circuit gain and pole-zero positions. For convenience in analysis, R_A and C_A represent the small-signal equivalent resistance and parasitic capacitance at node A, respectively. Clearly, $R_A=r_{o1}//R_1//r_{\pi 2}$, and C_A consists of the parasitic capacitance on the Q_1 collector, Q_2 base, and AC coupling capacitor C_1. From Fig. 4b, the DC voltage gain is derived as

$$A_{V0}=\frac{-g_{m1}R_A+\dfrac{1}{g_{m2}R_f}}{1+\dfrac{1}{g_{m2}r_{o3}}+\dfrac{1}{g_{m2}R_f}+\dfrac{1}{g_{m2}r_{o2}}}, \tag{1}$$

where g_{m1} and g_{m2} are the transconductances of Q_1 and Q_2, respectively, and r_{o2} and r_{o3} are the small-signal output impedances of Q_2 and Q_3, respectively. As both Q_2 and Q_3 are working in the active mode, $g_{m2}r_{o3}$>>1 and $g_{m2}r_{o2}$>>1. Accordingly, the following simplified gain expression can be obtained:

$$A_{V0}=\frac{1-g_{m1}R_A(1+g_{m2}R_f)}{1+g_{m2}R_f}. \tag{2}$$

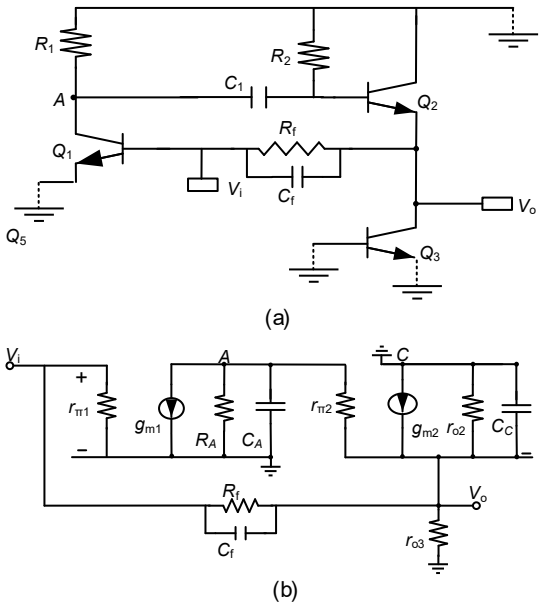

Fig. 4 Half circuit (a) and small-signal equivalent model (b)

From the amplifier gain specification, we have $g_{m1}R_A$>>1, and the amplifier's DC voltage gain is given as

$$A_{V0}=-g_{m1}R_A=-I_{C1}\frac{q}{kT}R_A, \tag{3}$$

where k is Boltzmann's constant, T is the Kelvin temperature, and q is the electron charge. Clearly, with a certain loading impedance R_A, the amplifier transconductance g_m can be tuned linearly with a biasing current. In other words, even without an accurate cryogenic device model, the required accurate gain can still be realized over a large temperature range using this proposed circuit structure.

2.3 Stability analysis

With the above gain expression, it can be seen that the dominant pole locates at node A. As a result, the 3-dB bandwidth $BW_{-3\,dB}$ can be derived as

$$BW_{-3\,dB}=\frac{1}{R_AC_A}. \tag{4}$$

Clearly, the amplifier gain is proportional to R_A. However, with a certain gain, the power consumption and the bandwidth of this proposed amplifier are inversely proportional to R_A. Accordingly, special attention should be paid to the amplifier gain, bandwidth, and power consumption issues.

To evaluate the stability of this amplifier, it is important to derive its input impedance Z_{in}:

$$Z_{in}=\frac{R_f}{1+g_{m1}(R_A\|C_A)}. \tag{5}$$

As indicated, the amplifier's input impedance is determined mainly by feedback resistor R_f and the gain. With a certain gain, the required input impedance can be derived by optimizing R_f. However, as the gain has the frequency roll-off characteristic, the input impedance increases with increasing frequency, thereby showing an inductive behavior. Typically, the SNSPD's output signal has the characteristic of a step signal, worsening the stability of the input and output signals. Typically, the rising time of the SNSPD is in the order of 100 ps. To solve these problems and reduce the variance of the input impedance to achieve better stability, a shunt capacitor C_f is introduced to be placed in parallel with R_f. Fig. 5 shows the effect of different C_f values on input impedance and input and output signals. Clearly, the input inductive impedance is suppressed with larger C_f, realizing input impedance matching across a wide frequency range. With a larger C_f, the stability of input and output signals is improved substantially. In this design, the shunt capacitor C_f is optimized to be 60 fF by taking into account the input impedance matching, stability, gain, and bandwidth. With further simulations, it is proved that the amplifier has good phase-frequency characteristics, making it possible to amplify the pulse signal with high fidelity.

3 Simulation and measurement results

Fig. 6a shows the die micrograph of the proposed amplifier, which is fabricated by a 0.13-μm BiCMOS process. Without using any inductor, and

excluding all the test pads, the chip active area is only about 0.43 mm×0.17 mm. As shown in Fig. 6b, the chip is bonded on a printed circuit board (PCB) with two sub-miniature-A (SMA) connectors for measurement purposes. The amplifier is measured under room and cryogenic temperatures, separately.

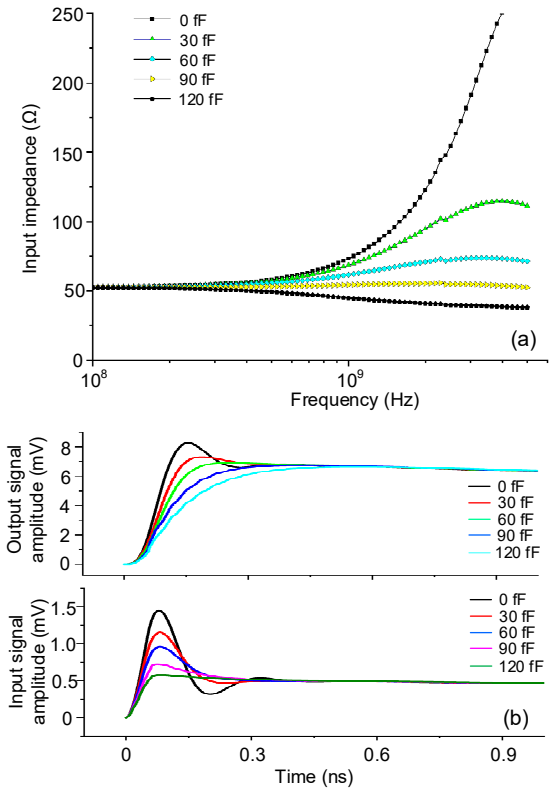

Fig. 5 Effect of C_f on the input impedance (a) and on the amplifier's output and input signal stability (b)

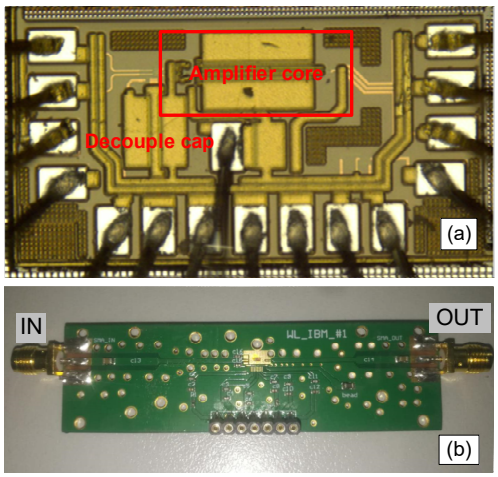

Fig. 6 Chip micrograph (a) and PCB board of the proposed cryogenic amplifier (b)

3.1 Room temperature performance

Using a network analyzer, the *S*-parameters of the amplifier are first measured at room temperature. To better illustrate the amplifier performance, the measurement and simulation results are compared (Fig. 7). From Fig. 7a, the amplifier gain in the passband range is about 21 dB, agreeing very well with the simulation results. At high frequencies, several discrepancies between simulation and test results arise. Because of the parasitic capacitances and loss from the PCB trace and bonding wire, the tested bandwidth is 1.13 GHz, which is lower than the simulation value of 1.32 GHz. Note that the gain fluctuation at 400 MHz is caused by the above resonance parameters. From Figs. 7b and 7c, the measured input and output return losses are lower than −10 dB over the frequency range of interest, agreeing well with the simulation results and showing that the amplifier has good terminal impedance matching performance. Fig. 7d compares the simulated S_{12} with the measured S_{12}. As indicated, S_{12} is lower than −30 dB, proving good isolation between the amplifier's input and output.

As the SNSPD's output signal amplitude is very small, high linearity performance is not critical for the SNSPD readout amplifier. To fully characterize the amplifier, it is better to use a pulse or step transient response to characterize the amplifier performance. However, limited by the test equipment, it is very difficult to provide a pulse signal with small amplitude and high SNR. In contrast, the sinusoidal signal from the equipment has high SNR even with very low signal amplitude. According to our experience, it is reasonable to use a sinusoidal drive to test the amplifier, as in He et al. (2019). To prove the effectiveness of this method, during the design the amplifier is simulated with the sinusoidal and pulse signals (Fig. 8). Figs. 8a and 8c show the input pulse signal and simulated output response, respectively. As indicated, the input and output signal amplitudes are 10 and 109 mV, respectively. For comparison, Figs. 8b and 8d show the input sinusoidal signal and simulated output response, respectively. As indicated, the input and output signal amplitudes are 10 and 104 mV, respectively. Clearly, with the pulse and sinusoidal input signals, the amplifier has high fidelity, and its gain agrees well with each other, proving the feasibility of the test with sinusoidal signals.

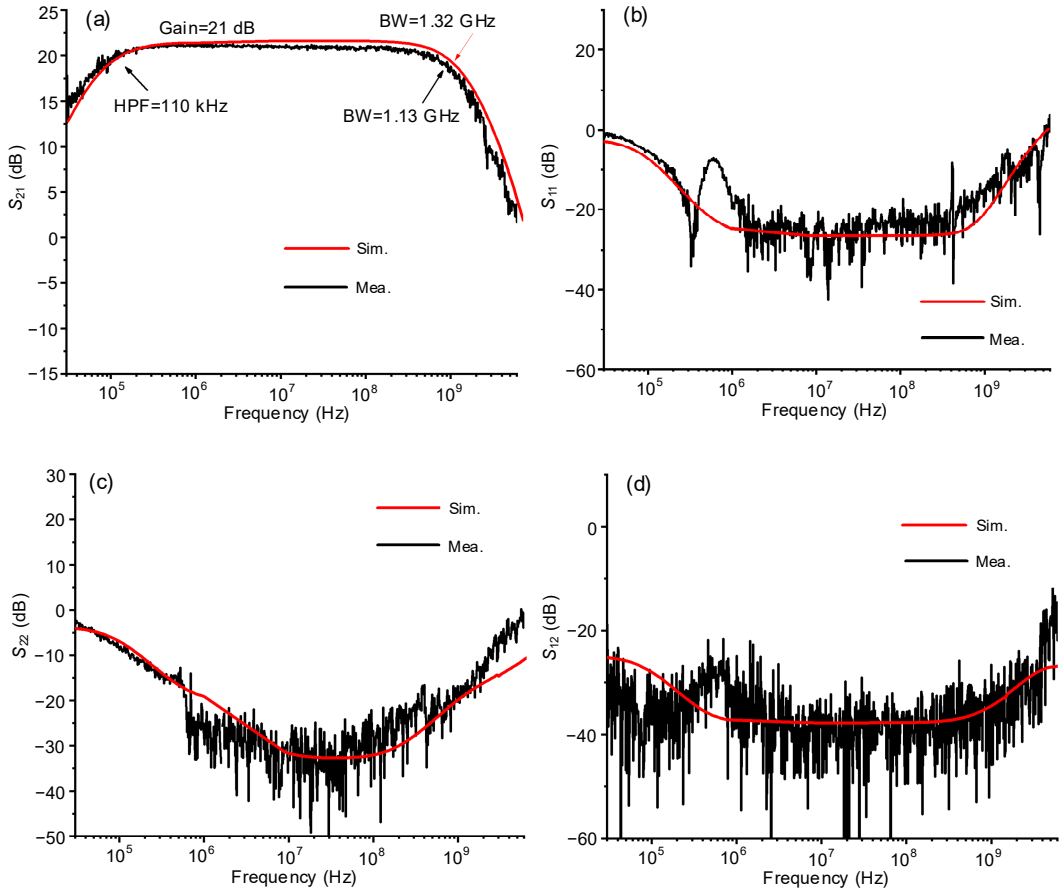

Fig. 7 The measured and simulated *S*-parameters at room temperature 300 K: (a) S_{21}; (b) S_{11}; (c) S_{22}; (d) S_{12}

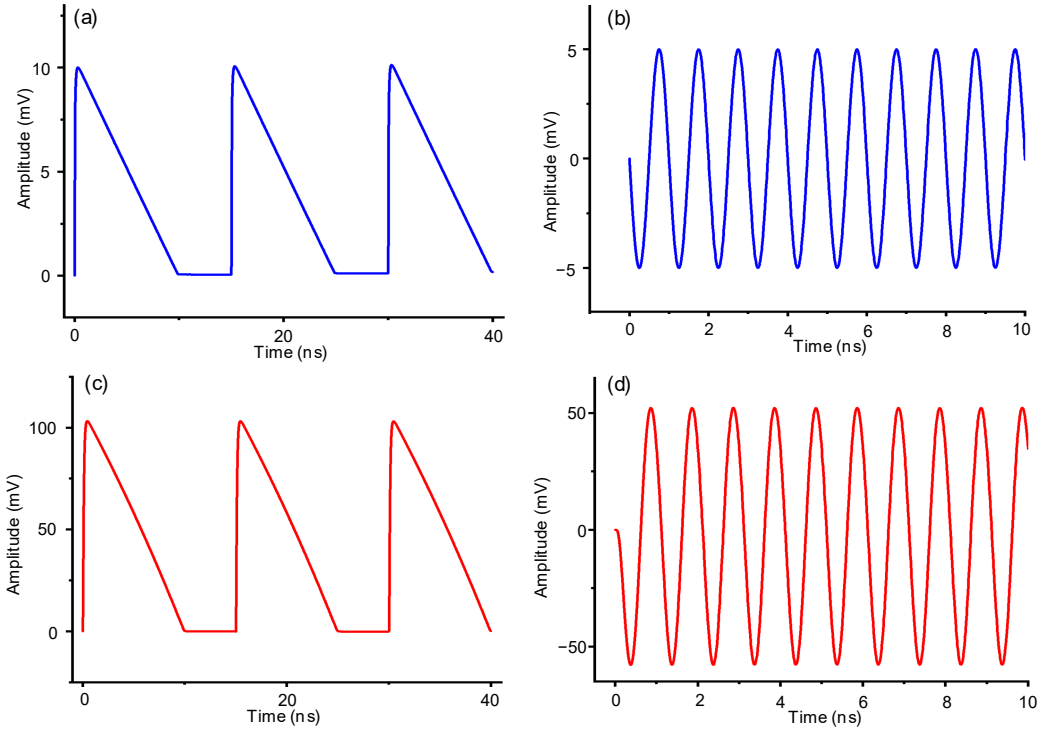

Fig. 8 Input pulse (a) and sinusoidal (b) signals and output pulse (c) and sinusoidal (d) responses

With a −50-dBm input sinusoidal signal at 100 MHz, Fig. 9 shows the transient output response signal. As indicated, its output signal amplitude is 20.88 mV_{pp}, translated into −29.6 dBm with a 50-Ω load. Accordingly, the calculated gain is about 20.4 dB, agreeing well with the *S*-parameter measurement result when taking into account the interconnecting line insertion loss. Fig. 10 shows the output signal when the input sinusoidal power and working frequency are increased to −35 dBm and 500 MHz, respectively. As indicated, with a 50-Ω load, the output voltage amplitude and power are 112.9 mV_{pp} and −14.9 dBm, respectively, agreeing with the simulated gain and proving that the amplifier is very stable. Further linearity measurements undertaken show that the amplifier has the input and output $P_{1\ dB}$ of about −29.4 and −9.4 dBm, respectively, meeting very well the system requirements.

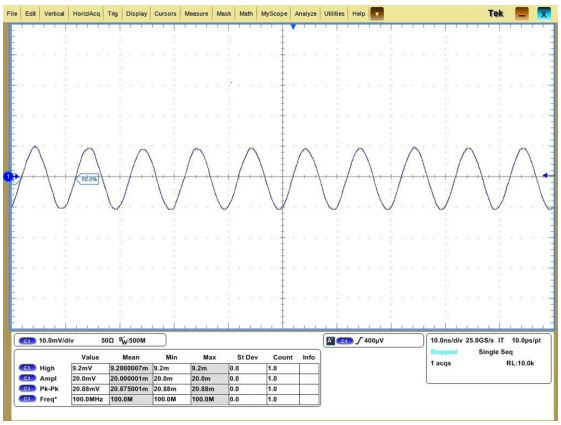

Fig. 9 Transient response of output with −50-dBm input at 100 MHz (300 K)

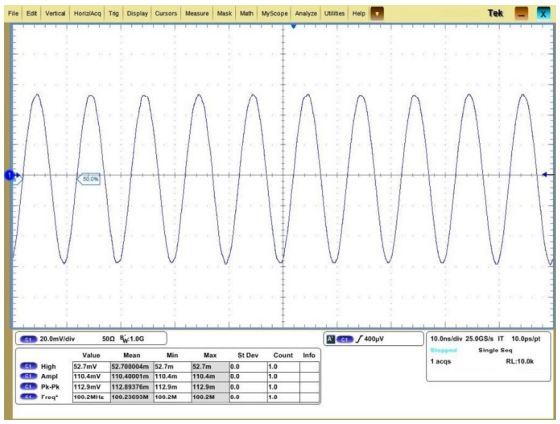

Fig. 10 Transient response of output with −35-dBm input at 500 MHz (300 K)

Because of the lack of a cryogenic device model, a noise simulation has been undertaken at room temperature (300 K) to optimize and evaluate the amplifier's noise performance. With simulations, the in-band noise density is less than $20\,\mathrm{nV}/\sqrt{\mathrm{Hz}}$. By integrating the noise power over the frequency band of interest, the output noise amplitude is about 0.9 mV. As mentioned before, the amplifier's typical output signal amplitude is about 3 mV, and the SNR is about 10.4 dB. According to Bardin and Weinreb (2008) and Montazeri et al. (2016), at the cryogenic temperature, e.g., 15 K, the transistor's noise performance will be improved by more than 15 times, thereby making it possible to meet the SNSPD readout requirements.

3.2 Cryogenic temperature performance

With the same measurement setup as in He et al. (2019), the cryogenic temperature performance of this amplifier is measured at 4.2 K. To obtain good RF performance, we use the tuning scheme in Section 2 to ensure that all the transistors have optimum DC operating points. In particular, as the transistor's turn-on voltage is higher at 4.2 K than at 300 K, to achieve a good input voltage headroom and high gain performance, the amplifier's biasing voltages V_b and V_{cc2} are increased to 0.4 and 2.5 V, respectively.

Table 1 summarizes the biasing conditions for the amplifier at room and cryogenic temperatures. Note that I_b is the current through biasing voltage V_b.

Table 1 Biasing conditions for the amplifier at room and cryogenic temperatures

Temp. (K)	V_{cc1} (V)	V_{cc2} (V)	V_b (V)	I_b (mA)
300	2	2.2	0.2	1.99
4.2	2	2.5	0.4	0.70

Fig. 11 shows the measured S_{21} of the amplifier with varying biasing current source I_s. When I_s is increased from 60 to 300 μA, the amplifier gain is improved from 15 to 24 dB. With a 150-μA biasing current, the amplifier's power consumption is only 3.1 mW. With such a biasing current, Fig. 12 shows all the measured *S*-parameters. As indicated, the amplifier gain is 20.5 dB and its −3-dB bandwidth is from 120 kHz to 1.3 GHz. For better performance comparison, the measured *S*-parameters at room and cryogenic temperatures are compared, indicating

good agreement. Note that, different from the test results at room temperature, the amplifier gain fluctuates at 200 kHz and 460 MHz. This is caused by the effect of cryogenic temperature on parasitic capacitance, thus changing its resonant frequencies. As illustrated in Figs. 12b–12d, over the frequency range of interest, both the input and output return losses of the amplifier are less than −10 dB, and S_{12} of the amplifier is better than −30 dB.

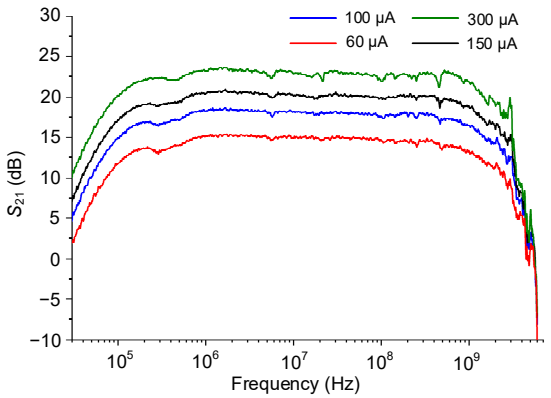

Fig. 11 Measured S_{21} with different biasing currents at 4.2 K

Linearity and noise tests are not performed at cryogenic temperature because of the limitations of the test equipment. To evaluate the amplifier performance, transient measurements are performed with large and small sinusoidal signals. With a 500-MHz −40-dBm input sinusoidal signal, transient measurements are undertaken at 4.2 K. Fig. 13 shows a 68-mV output transient signal. As indicated, the signal quality is quite high, showing neither compression nor resonance issue and proving that the amplifier is very reliable and stable. As indicated in Fig. 14, when the input signal power is −57 dBm, with amplitude lower than 1 mV_{pp}, the amplifier's output signal amplitude is 9.6 mV_{pp}. Clearly, taking into account the supply and environment, the output signal is very clear, showing very good SNR and meeting typical SNSPD readout requirements.

Table 2 summarizes the state-of-the-art cryogenic amplifiers operating within the GHz frequency range. Clearly, this work achieves very good electrical performance and high area efficiency without using any inductor. Moreover, the low corner frequency of the −3-dB bandwidth (i.e., low cut-off frequency) is the lowest among all the references in Table 2.

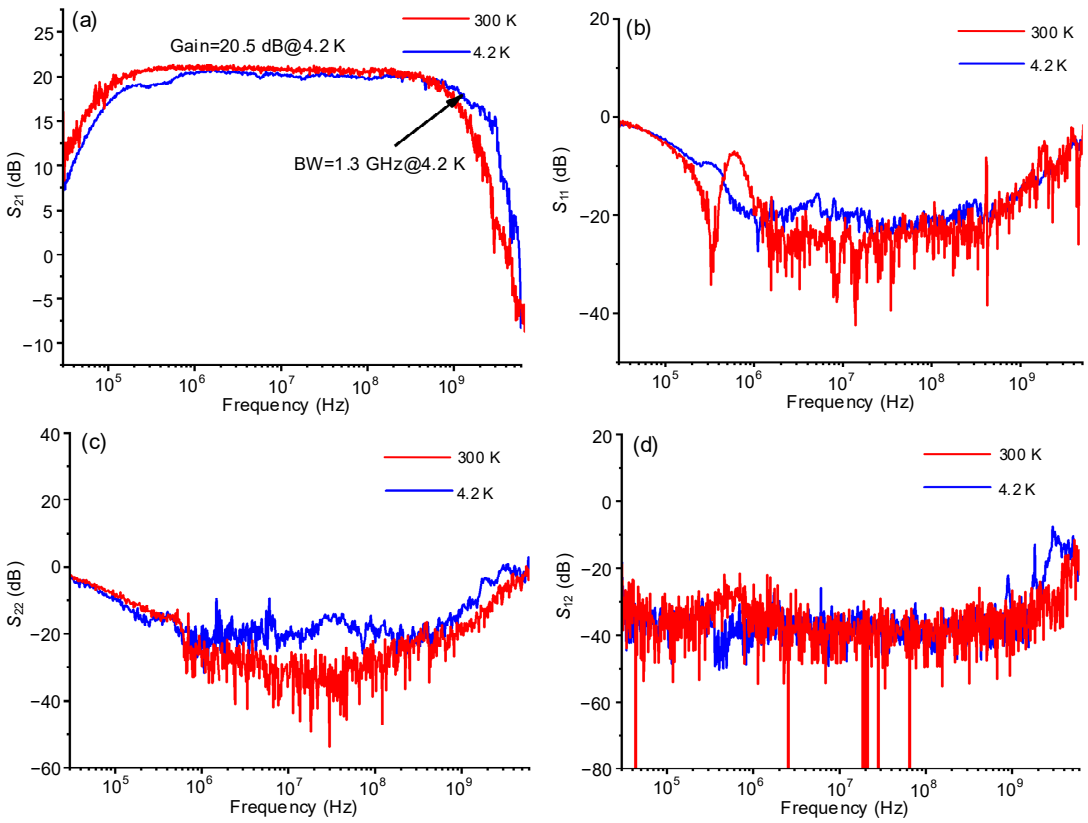

Fig. 12 Measured *S*-parameters at 4.2 K and 300 K: (a) S_{21}; (b) S_{11}; (c) S_{22}; (d) S_{12}

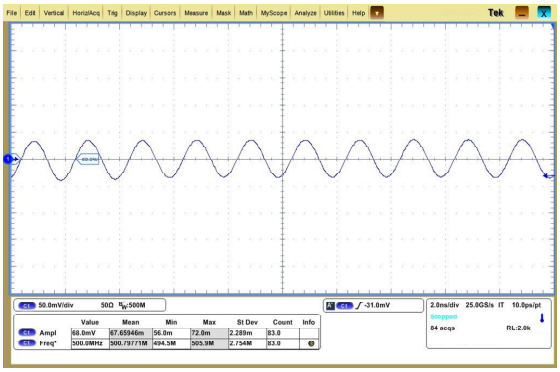

Fig. 13 The 68-mV 500-MHz output sinusoidal signal at 4.2 K

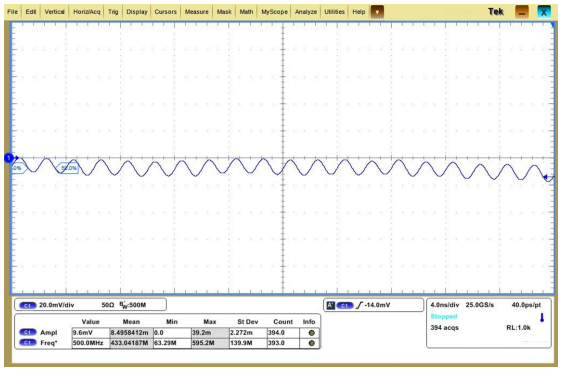

Fig. 14 The 9.6-mV 500-MHz output sinusoidal signal at 4.2 K

Table 2 Comparison with state-of-the-art cryogenic amplifiers

Reference	Technology	Gain (dB)	BW (GHz)	$f_{-3\ \mathrm{dB,\ low}}$ (MHz)	P_{diss} (mW)	Area (mm^2)
Bardin and Weinreb (2009)	SiGe HBT	29.6	4.9	100	20.0	0.3
Shiao et al. (2014)	SiGe HBT	10.0	3.4	600	13.5	0.3
Chang and Bardin (2017)	SiGe HBT	22.0	2.7	300	32.0	0.6
Korolev et al. (2016)	GaAs	29.0	1.0	50	4.0	N/A
He et al. (2019)	SiGe HBT	23.0	3.4	0.13	4.3	0.5 (0.075)*
This work	SiGe HBT	20.5	1.3	0.12	3.1	0.5 (0.073)*

*The value in the brackets represents the active area of the chip

In addition, the power consumption of this amplifier is only 1/8–1/4 that of Bardin and Weinreb (2009), Shiao et al. (2014), and Chang and Bardin (2017). Compared to He et al. (2019), the power consumption of this amplifier is reduced by about 28%, relaxing substantially the cooling power requirements.

4 Conclusions

In this study, a low-power inductorless wideband cryogenic amplifier for a superconducting nanowire single-photon detector was produced using a 0.13-μm SiGe BiCMOS process. By highlighting the relationship between the gain and the tunable design parameters, this amplifier can operate at temperatures from 300 to 4.2 K with adjustable DC biasing points. To achieve a flat terminal impedance over the frequency range of interest, an RC shunt compensation structure was introduced, improving the amplifier's closed-loop stability and suppressing the amplifier overshoot. The *S*-parameters and transient performance were measured at room temperature (300 K) and cryogenic temperature (4.2 K), separately. With good input and output matching, the measurement results showed that the amplifier achieved a 21-dB gain with a 3-dB bandwidth of 1.13 GHz at 300 K. At 4.2 K, the gain of the amplifier can be tuned from 15 to 24 dB, achieving a 3-dB bandwidth spanning from 120 kHz to 1.3 GHz and consuming only 3.1 mW. Over the whole 3-dB bandwidth range, the amplifier's input and output return losses were better than 10 dB.

Contributors

Lianming LI and Long HE proposed the idea, designed the research, and drafted the paper. Xiaokang NIU helped design the circuit and processed the data. Xu WU helped organize the paper. Xu WU, Chao WAN, Lin KANG, Xiaoqing JIA, Labao ZHANG, Qingyuan ZHAO, and Xuecou TU revised the paper. Lianming LI and Long HE revised and finalized the paper.

Compliance with ethics guidelines

Lianming LI, Long HE, Xu WU, Xiaokang NIU, Chao WAN, Lin KANG, Xiaoqing JIA, Labao ZHANG, Qingyuan ZHAO, and Xuecou TU declare that they have no conflict of interest.

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